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PATENT APPLICATION

ATTORNEY DOCKET NO. 10014282-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	**Andrew Spencer**	**Confirmation No.:**	**3876**
Application No.:	**10/689,244**	**Examiner:**	**Chun Cao**
Filing Date:	**Oct. 20, 2003**	**Group Art Unit:**	**2115**

Title: SYSTEM AND METHOD FOR SETTING A CLOCK RATE OF A MEMORY CARD

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on Nov. 13, 2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500 . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

Andrew Spencer

By /Christopher P. Kosh/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Andrew Spencer	Examiner:	Chun Cao
Serial No.:	10/689,244	Group Art Unit:	2115
Filed:	Oct. 20, 2003	Docket No.:	10014282-1
Due Date:	Jan. 13, 2007		

Title: SYSTEM AND METHOD FOR SETTING A CLOCK RATE OF A MEMORY CARD

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on November 13, 2006, appealing the final rejection of claims 1-36 of the above-identified application as set forth in the Final Office Action mailed September 15, 2006.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $500.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. § 41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-36.

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REAL PARTY IN INTEREST

The intellectual property embodied in the pending application is assigned to Hewlett-Packard Development Company, L.P.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed September 15, 2006, claims 1-36 were finally rejected. Claims 1-36 are pending in the application. Claims 1-36 are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments were filed subsequent to the Final Office Action mailed September 15, 2006.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Discussions about elements of independent claims 1, 10, 19, 28, and 33 can be found at least at the cited locations in the specification and drawings.

Independent claim 1 claims a memory card. The memory card includes a buffer configured to receive transactions, a storage media, a control circuit coupled to the buffer and the storage media, and a processor system coupled to the control circuit. The processor system is configured to detect a rate of transactions received by the buffer. The control circuit is configured to cause a first clock signal to be provided to the buffer and the storage media at a first clock rate that varies in dependence on the detected rate of the transactions. (See, e.g., page 3, lines 6-9 and 20-22; page 6, lines 3-5 and 14-16; page 7, lines 1-4, 11-14, and 23; Figure 1, reference numbers 120, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120).

Independent claim 10 claims a system. The system includes a host device and a memory card configured to couple to the host device. The memory card includes a storage

media. The memory card is configured to provide a first clock signal to the storage media at a first clock rate that varies in dependence on a number of transactions received by the memory card from the host device during a time period. (See, e.g., page 2, lines 25-31; page 3, lines 6-9 and 20-22; page 6, lines 3-5 and 14-16; page 7, lines 1-4, 11-14, and 23; Figure 1, reference numbers 110, 120, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120 and 310).

Independent claim 19 claims a method. A first rate of transactions received by a buffer in a memory card is determined. A first clock signal of the memory card is set to a first clock rate that varies in dependence on the rate of transactions. The first clock signal is provided to the buffer and a storage media in the memory card. (See, e.g., page 3, lines 6-9 and 20-22; page 6, lines 3-5 and 14-16; page 7, lines 1-4, 11-14, and 23; Figure 1, reference numbers 120, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120).

Independent claim 28 claims a memory card. The memory card includes a buffer configured to receive transactions, a storage media, a clock configured to generate a clock signal and provide the clock signal to the buffer and the storage media, a means for determining a rate of the transactions received by the buffer, and a means for causing the clock signal to be set at a rate associated with the rate of transactions. (See, e.g., page 3, lines 6-9 and 20-22; page 4, lines 20-23; page 6, lines 3-5 and 14-16; page 7, lines 1-4, 11-14, and 23; Figure 1, reference numbers 120, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120).

Independent claim 33 claims a memory card. The memory card includes a buffer, an interface configured to receive transactions from a host device and provide the transactions to the buffer, a storage media, a control circuit coupled to the buffer and the storage media, and a processor system coupled to the control circuit. The processor system is configured to detect a rate of transactions received by the buffer. The processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the rate of transactions received by the buffer. The control circuit is configured to cause the first clock signal to be provided to the buffer and the storage media. (See, e.g., page 3, lines 6-9 and 18-22; page 4, lines 20-23; page 6, lines 3-5 and 14-16; page

7, lines 1-4, 11-14, and 23; Figure 1, reference numbers 120, 132, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,407,940 to Aizawa et al. ("Aizawa") in view of U.S. Patent No. 6,157,646 to Yu et al. ("Nichols").

ARGUMENT

I. The Applicable Law

The Examiner has the burden under 35 U.S.C. §103 to establish a *prima facie* case of obviousness. *In re Fine,* 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *Id.* Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Third, the prior art reference or combined prior art references must teach or suggest all of the claim limitations. *In re Royka,* 490 F.2d 981, 180 USPQ 580 (CCPA 1974). These three criteria are also set forth in §706.02(j) of the M.P.E.P. In performing the obviousness inquiry under 35 U.S.C. §103, the Examiner must avoid hindsight. *In re Bond,* 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied,* 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990).

II. Rejection of Claims 1-36 under 35 U.S.C. § 103(a) as being unpatentable over Aizawa in view of Nichols.

The Examiner rejected claims 1-36 under 35 U.S.C. §103(a) as being unpatentable over Aizawa in view of Nichols. Appellants respectfully submit that the Examiner has not established a *prima facie* case of obviousness of each of the independent 1, 10, 19, 28, and 33, and the claims depending therefrom.

A. Rejection of Claim 1 under 35 U.S.C. §103(a) as being unpatentable over Aizawa in view of Nichols.

Independent claim 1 is directed to a "memory card" and recites the following:

(a) "a buffer configured to receive transactions";

(b) "a storage media";

(c) "a control circuit coupled to the buffer and the storage media";

(d) "a processor system coupled to the control circuit"; and

(e) "wherein the processor system is configured to detect a rate of transactions received by the buffer, and wherein the control circuit is configured to cause a first clock signal to be provided to the buffer and the storage media at a first clock rate that varies in dependence on the detected rate of the transactions."

Aizawa discloses a memory card device that is designed to be removably inserted in a host apparatus. (Aizawa at col. 1, lines 63-64). The memory card device includes a nonvolatile memory device, a controller configured to execute commands supplied from the host apparatus, thereby to write data into, and read data from, the nonvolatile memory, a clock signal generator that includes a phase locked loop (PLL) configured to generate a clock signal to be supplied to the controller, and a clock control unit configured to operate in a first clock control mode and a second clock control mode. (Aizawa at col. 1, line 64-col. 2, line 15). Aizawa explicitly relates to a memory card device that can be used in various types of electronic apparatuses. (Aizawa at col. 1, lines 13-14).

Nichols discloses a circuit and method for synchronizing a service clock at a destination node with a service clock at a source node for circuit emulation service over a packet network. (Nichols at Abstract). The circuit and method described in Nichols uses a direct digital synthesis (DDS) circuit that is set based on analysis of a large sample of synchronous residual time stamp (RTS) values. (Nichols at col. 2, lines 37-40). Further, buffer fill levels at the destination node are simultaneously monitored and information derived from this data is used to adjust the setting of the DDS circuit, at an optimum buffer fill level. (Nichols at col. 2, lines 40-43). Nichols explicitly relates to the field of telecommunications. (Nichols at col. 1, lines 5-6).

The Examiner, citing Figure 1, col. 3, lines 22-25, col. 4, lines 33-35, col. 5, lines 25-34 and 48-49 of Aizawa, argues that Aizawa discloses "a buffer configured to receive

transactions," "a storage media," "a control circuit coupled to the buffer and the storage media," "a processor system coupled to the control circuit," and "wherein the control circuit is configured to cause a first clock signal to be provided to the buffer and the storage media at a first clock rate...." (Final Office Action at page 2). The Examiner admits that Aizawa does not explicitly disclose "wherein the processor system is configured to detect a rate of transactions received by the buffer" (emphasis added) and "wherein the control circuit is configured to cause a first clock signal to be provided to the buffer at the storage media at a first clock rate that varies in dependence on the detected rate of the transactions," (emphasis added) both as claimed in claim 1. (Final Office Action at page 2). The Examiner, citing Figure 1, col. 4, lines 16-19 and 52-53, and col. 4, line 67-col. 5, line 2 of Nichols, argues that Nichols discloses the recited limitations not disclosed in Aizawa. (Final Office Action at pages 2-3). The Examiner then states, without citation to either of the references, that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention [sic] to combine the teachings of Aizawa and Nichols because the specify [sic] teachings of Nichols stated above would improve the performance of Aizawa system [sic] adjusting the clock signal corresponding a data transmission rate [sic] to reduce power consumption of the memory card." (Final Office Action at page 3). Appellants respectfully disagree.

Aizawa and Nichols, either alone or in combination, do not teach or suggest a "memory card" that includes a processor system "wherein the processor system is configured to detect a rate of transactions received by the buffer, and wherein the control circuit is configured to cause a first clock signal to be provided to the buffer and the storage media at a first clock rate that varies in dependence on the detected rate of the transactions" as claimed in claim 1 (emphasis added). While the Examiner argues that Nichols discloses the recited limitations of claim 1 which are not disclosed by Aizawa, Nichols does not teach or suggest a memory card whatsoever, much less a memory card including a processor system and control circuit as configured and claimed in claim 1.

Further, Nichols is directed to synchronizing a service clock at a destination node 100, which is a very specific telecommunications application. (Nichols at Abstract). The microcontroller 116 and data frame buffer 114 of Nichols are part of a destination node 100, which receives data packets from source node 104 over a packet network 102. (Nichols at Figure 1 and col. 3 lines 38-40). Appellants respectfully submit that Nichols is unrelated to

the claimed memory card and that one of ordinary skill in the art interested in improving memory cards would not look to telecommunications art involving synchronizing a service clock for a solution *See In re Wood*, 599 F.2d 1032, 1036, 202 USPQ 171, 174 (CCPA 1979) (noting that in determining whether a reference is non-analogous art, first decide whether the reference is in the inventor's field of endeavor, and if not, determine whether the reference is reasonably pertinent to the particular problem with which the inventor was involved).

The Examiner has provided no citations to either Aizawa or Nichols to support combining the cited references in the manner proposed by the Examiner. The Federal Circuit has stated that "there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention." *Karsten Manufacturing Corp. v. Cleveland Golf Co.*, 58 U.S.P.Q.2d 1286, 1293 (Fed. Cir. 2001). The Examiner's conclusory statement that combining Aizawa and Nichols would improve the performance of the Aizawa system amounts to nothing more than conjecture and impermissible hindsight reconstruction.

Aizawa discloses a secured digital (SD) memory card 11 that can be inserted into, and removed from, a card slot made in the host apparatus 12. (Aizawa at col. 3 , lines 7-8). In contrast, Nichols discloses a destination node 100 that receives data packets from source node 104 over packet network 102. (Nichols at col. 3, lines 38-40). By teaching that data is transferred by inserting the memory card 11 into the card slot of host apparatus 12, Aizawa teaches away from transferring data between the memory card 11 and the host apparatus 112 over a network. Indeed, modifying Aizawa such that data can be transferred between the memory card 11 and the host apparatus 12 over a network would change the principle operation of Aizawa, require substantial reconstruction and redesign of the memory card 11 and the host apparatus 12, and effectively render the card slot in the host apparatus 12 inoperable.

The MPEP states that a *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997). The MPEP further states that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." MPEP §2143.01,

citing *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). The MPEP also states that, in the *Ratti* case, "[t]he court reversed the rejection holding the 'suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary reference] construction was designed to operate." MPEP §2143.01, citing *In re Ratti*, 270 F.2d at 813, 123 USPQ at 352.

In view of the above, each and every limitation of independent claim 1 is not taught or suggested by Aizawa and Nichols, either alone or in combination. Further, the Examiner has offered no source of suggestion, motivation or teaching in Aizawa or Nichols, other than hindsight knowledge, to select and combine the disparate teachings Aizawa and Nichols. Aizawa teaches away from Nichols. In addition, combining Aizawa and Nichols would change the principle of operation of the system of Aizawa, require a substantial reconstruction and redesign of the system of Aizawa, and render at least parts of the system of Aizawa inoperable. Accordingly, because the Examiner has not established a *prima facie* case of obviousness of claim 1, the rejection of independent claim 1 and dependent claims 2-9 under 35 U.S.C. § 103(a) should be reversed.

B. Rejection of Claim 10 under 35 U.S.C. §103(a) as being unpatentable over Aizawa in view of Nichols.

Independent claim 10 is directed to a "system" and recites the following:

(a) "a host device";

(b) "a memory card configured to couple to the host device"; and

(c) "wherein the memory card includes a storage media, wherein the memory card is configured to provide a first clock signal to the storage media at a first clock rate that varies in dependence on a number of transactions received by the memory card from the host device during a time period."

The Examiner, citing Figure 1, col. 5, lines 30-34 and 48-49 of Aizawa, argues that Aizawa discloses "a host device," "a memory card configured to couple to the host device," and "wherein the memory card includes a storage media, wherein the memory card is configured to provide a first clock signal to the storage media at a first clock rate...." (Final Office Action at page 4). The Examiner admits that Aizawa does not disclose "wherein the

memory card is configured to provide a first clock signal to the storage media at a first clock rate that varies in dependence on a number of transactions received by the memory card from the host device during a time period" as claimed in claim 10 (emphasis added). (Final Office Action at page 5). The Examiner, citing Figure 1, col. 4, lines 16-19 and 52-53, and col. 4, line 64-col. 5, line 8 of Nichols, argues that Nichols discloses the recited limitations not disclosed in Aizawa. (Final Office Action at page 5). The Examiner then states, without citation to either of the references, that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention [sic] to combine the teachings of Aizawa and Nichols because the specify [sic] teachings of Nichols stated above would improve the performance of Aizawa system [sic] adjusting the clock signal corresponding a data transmission rate [sic] to reduce power consumption of the memory card." (Final Office Action at page 5). Appellants respectfully disagree.

Aizawa and Nichols, either alone or in combination, do not teach or suggest a system that includes a "memory card configured to couple to the host device" and "wherein the memory card is configured to provide a first clock signal to the storage media at a first clock rate that varies in dependence on a number of transactions received by the memory card from the host device during a time period," as claimed in claim 10 (emphasis added). While the Examiner argues that Nichols discloses the recited limitations of claim 10 which are not disclosed by Aizawa, Nichols does not teach or suggest a system including a memory card whatsoever, much less a system including a memory card as configured and claimed in claim 10.

Further, Nichols is directed to synchronizing a service clock at a destination node 100, which is a very specific telecommunications application. (Nichols at Abstract). The microcontroller 116 and data frame buffer 114 of Nichols are part of a destination node 100, which receives data packets from source node 104 over a packet network 102. (Nichols at Figure 1 and col. 3 lines 38-40). Appellants respectfully submit that Nichols is unrelated to the claimed system and that one of ordinary skill in the art interested in improving systems including memory cards would not look to telecommunications art involving synchronizing a service clock for a solution *See In re Wood*, 599 F.2d 1032, 1036, 202 USPQ 171, 174 (CCPA 1979) (noting that in determining whether a reference is non-analogous art, first decide whether the reference is in the inventor's field of endeavor, and if not, determine

whether the reference is reasonably pertinent to the particular problem with which the inventor was involved).

The Examiner has provided no citations to either Aizawa or Nichols to support combining the cited references in the manner proposed by the Examiner. The Federal Circuit has stated that "there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention." *Karsten Manufacturing Corp. v. Cleveland Golf Co.*, 58 U.S.P.Q.2d 1286, 1293 (Fed. Cir. 2001). The Examiner's conclusory statement that combining Aizawa and Nichols would improve the performance of the Aizawa system amounts to nothing more than conjecture and impermissible hindsight reconstruction.

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The MPEP states that a *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997). The MPEP further states that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." MPEP §2143.01, citing *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). The MPEP also states that, in the *Ratti* case, "[t]he court reversed the rejection holding the 'suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary

reference] construction was designed to operate." MPEP §2143.01, citing *In re Ratti*, 270 F.2d at 813, 123 USPQ at 352.

In view of the above, each and every limitation of independent claim 10 is not taught or suggested by Aizawa and Nichols, either alone or in combination. Further, the Examiner has offered no source of suggestion, motivation or teaching in Aizawa or Nichols, other than hindsight knowledge, to select and combine the disparate teachings Aizawa and Nichols. Aizawa teaches away from Nichols. In addition, combining Aizawa and Nichols would change the principle of operation of the system of Aizawa, require a substantial reconstruction and redesign of the system of Aizawa, and render at least parts of the system of Aizawa inoperable. Accordingly, because the Examiner has not established a *prima facie* case of obviousness of claim 10, the rejection of independent claim 10 and dependent claims 11-18 under 35 U.S.C. § 103(a) should be reversed.

C. Rejection of Claim 19 under 35 U.S.C. §103(a) as being unpatentable over Aizawa in view of Nichols.

Independent claim 19 is directed to a "method" and recites "determining a first rate of transactions received by a memory card" and "setting a first clock signal of the memory card to a first clock rate that varies in dependence on the rate of transactions." The Examiner argues that "Aizawa and Nichols together teaches [sic] the claimed system[, and therefore,] Aizawa and Nichols together teach the claimed method of steps to carry out the claimed system." (Final Office Action at page 7).

Appellants respectfully submit that the Examiner has not established a *prima facie* case of obviousness for claim 19 for at least the reasons provided for claim 1 in subsection A above. Accordingly, the rejection of independent claim 19 and dependent claims 20-27 under 35 U.S.C. § 103(a) should be reversed.

D. Rejection of Claim 28 under 35 U.S.C. §103(a) as being unpatentable over Aizawa in view of Nichols.

Independent claim 28 is directed to a "memory card" and recites the following:

(a) "a buffer configured to receive transactions";

(b) "a storage media";

(c) "a clock configured to generate a clock signal and provide the clock signal to the buffer and the storage media";

(d) "means for determining a rate of the transactions received by the buffer"; and

(e) "means for causing the clock signal to be set at a rate associated with the rate of transactions."

Without addressing the specific limitations of claim 28, the Examiner argues that "claims 28-36 are written in means plus functions and contained [sic] the same limitations as claims 1-9." It is unclear why the Examiner makes such a blanket statement as claim 28 clearly contains limitations not found in claims 1-9. In particular, claim 28 claims "a clock configured to generate a clock signal and provide the clock signal to the buffer and the storage media." By not addressing each and every limitation of claim 28, the Examiner necessarily has not made out a *prima facie* case of obviousness.

Notwithstanding the foregoing, Appellants respectfully submit that Aizawa and Nichols, either alone or in combination, do not teach or suggest "means for determining a rate of the transactions received by the buffer" and "means for causing the clock signal to be set at a rate associated with the rate of transactions" as claimed in claim 28 for at least the reasons presented for claim 1 in subsection A above.

In view of the above, each and every limitation of independent claim 28 is not taught or suggested by Aizawa and Nichols, either alone or in combination. Accordingly, because the Examiner has not established a *prima facie* case of obviousness of claim 28, the rejection of independent claim 28 and dependent claims 29-32 under 35 U.S.C. § 103(a) should be reversed.

E. Rejection of Claim 33 under 35 U.S.C. §103(a) as being unpatentable over Aizawa in view of Nichols.

Independent claim 33 is directed to a "memory card" and recites the following:

(a) "a buffer";

(b) "an interface configured to receive transactions from a host device and provide the transactions to the buffer";

(c) "a storage media";

(d) "a control circuit coupled to the buffer and the storage media";

(e) "a processor system coupled to the control circuit";

(f) "wherein the processor system is configured to detect a rate of transactions received by the buffer, wherein the processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the rate of transactions received by the buffer, and wherein the control circuit is configured to cause the first clock signal to be provided to the buffer and the storage media."

Without addressing the specific limitations of claim 28, the Examiner argues that "claims 28-36 are written in means plus functions and contained [sic] the same limitations as claims 1-9." The Examiner's statement is incorrect for at least two reasons. First, nothing in claims 33-36 indicate the use of means plus function claiming. Second, it is unclear why the Examiner makes such a blanket statement as claim 33 clearly contains limitations not found in claims 1-9. In particular, claim 33 claims "an interface configured to receive transactions from a host device and provide the transactions to the buffer" and "wherein the processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the rate of transactions received by the buffer." (Emphasis added.) By not addressing each and every limitation of claim 33, the Examiner necessarily has not made out a *prima facie* case of obviousness.

Notwithstanding the foregoing, Appellants respectfully submit that Aizawa and Nichols, either alone or in combination, do not teach or suggest "wherein the processor system is configured to detect a rate of transactions received by the buffer, wherein the processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the rate of transactions received by the buffer, and wherein the control circuit is configured to cause the first clock signal to be provided to the buffer and the storage media" as claimed in claim 33 for at least the reasons provided in claim 1 in subsection A above.

In view of the above, each and every limitation of independent claim 33 is not taught or suggested by Aizawa and Nichols, either alone or in combination. Accordingly, because the Examiner has not established a *prima facie* case of obviousness of claim 33, the rejection of independent claim 33 and dependent claims 34-36 under 35 U.S.C. § 103(a) should be reversed.

CONCLUSION

For the above reasons, Appellants respectfully submit that the cited references do not render obvious claims of the pending Application. The pending claims distinguish and are non-obvious over the cited references, and therefore, Appellants respectfully submit that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-36 be allowed.

Any inquiry regarding this Response should be directed to Wendell J. Jones at Telephone No. (408) 938-0980, Facsimile No. (650) 852-8063 or Christopher P. Kosh at Telephone No. (512) 241-2403, Facsimile No. (512) 241-2409. In addition, all correspondence should continue to be directed to the following address:

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Dated: January 11, 2007
CPK:dmd

__/Christopher P. Kosh/_____
Christopher P. Kosh
Reg. No. 42,760

CLAIMS APPENDIX

1. (Previously Presented) A memory card comprising:

a buffer configured to receive transactions;

a storage media;

a control circuit coupled to the buffer and the storage media; and

a processor system coupled to the control circuit;

wherein the processor system is configured to detect a rate of transactions received by the buffer, and wherein the control circuit is configured to cause a first clock signal to be provided to the buffer and the storage media at a first clock rate that varies in dependence on the detected rate of the transactions.

2. (Previously Presented) The memory card of claim 1 wherein the processor system is configured to cause the control circuit to set the first clock signal to the first clock rate associated with the rate of transactions received by the buffer.

3. (Original) The memory card of claim 2 further comprising:

a buffer management circuit;

wherein the buffer management circuit is configured to provide information to the processor system, and wherein the processor system is configured to determine the rate of transactions received by the buffer using the information.

4. (Original) The memory card of claim 2 further comprising:

a master clock configured to provide a second clock signal at a second clock rate to the processor system and the control circuit;

wherein the control circuit is configured to generate the first clock signal using the second clock signal.

5. (Original) The memory card of claim 4 wherein the first clock rate differs from the second clock rate.

6. (Original) The memory card of claim 1 further comprising:

a first interface coupled to the buffer and configured to receive the transactions from a host device and provide the transactions to the buffer; and

a second interface coupled to the buffer and the storage media.

7. (Original) The memory card of claim 1 wherein the transactions include read transactions configured to cause information to be read from the storage media.

8. (Original) The memory card of claim 1 wherein the transactions include write transactions configured to cause information to be written to the storage media.

9. (Original) The memory card of claim 1 wherein the transactions include read transactions configured to cause information to be read from the storage media and write transactions configured to cause information to be written to the storage media.

10. (Original) A system comprising:

a host device; and

a memory card configured to couple to the host device;

wherein the memory card includes a storage media, wherein the memory card is configured to provide a first clock signal to the storage media at a first clock rate that varies in dependence on a number of transactions received by the memory card from the host device during a time period.

11. (Original) The system of claim 10 wherein the memory card includes a processor system and a control circuit coupled to the processor system, wherein the processor system is configured to determine the number of transactions received by the memory card from the host device during the time period, and wherein the processor system is configured to cause the control circuit to set the rate of the first clock signal in response to the number of transactions.

12. (Original) The system of claim 11 wherein the memory card includes a buffer and a buffer management circuit, wherein the buffer management circuit is configured to provide

information to the processor system, and wherein the processor system is configured to determine the number of transactions received by the memory card during the time period using the information.

13. (Original) The system of claim 11 wherein the memory card includes a clock configured to provide a second clock signal to the processor system and the control circuit at a second clock rate, and wherein the control circuit is configured to generate the first clock signal using the second clock signal.

14. (Original) The system of claim 10 wherein host device comprises a digital camera.

15. (Original) The system of claim 10 wherein the memory card includes a buffer and an interface coupled to the buffer, and wherein the interface is coupled to receive the transactions from the host device and provide the transactions to the buffer.

16. (Original) The system of claim 10 wherein the transactions include read transactions configured to cause information to be read from the memory card and provided to the host device.

17. (Original) The system of claim 10 wherein the transactions include write transactions configured to cause information to be written from the host device to the memory card.

18. (Original) The system of claim 10 wherein the transactions include read transactions configured to cause first information to be read from the storage media and provided to the host device and write transactions configured to cause second information to be written from the host device to the memory card.

19. (Previously Presented) A method comprising:

determining a first rate of transactions received by a buffer in a memory card;

setting a first clock signal of the memory card to a first clock rate that varies in dependence on the rate of transactions; and

providing the first clock signal to the buffer and a storage media in the memory card.

20. (Previously Presented) The method of claim 19 further comprising:

determining the first rate of transactions by monitoring the buffer of the memory card.

21. (Previously Presented) The method of claim 19 further comprising:

determining the first rate of transactions by monitoring a number of times the buffer of the memory card fills over a time period.

22. (Previously Presented) The method of claim 19 further comprising:

determining the first rate of transactions by monitoring a number of times the buffer of the memory card empties over a time period.

23. (Original) The method of claim 19 further comprising:

determining the first rate of transactions by comparing to a threshold level the amount of information stored in the buffer.

24. (Original) The method of claim 19 further comprising:

subsequent to determining the first rate, determining a second rate of transactions received by the memory card; and

setting the first clock signal to a second clock rate associated with the rate of transactions.

25. (Original) The method of claim 19 wherein the transactions include read transactions configured to cause information to be read from the memory card.

26. (Original) The method of claim 19 wherein the transactions include write transactions configured to cause information to be written to the memory card.

27. (Original) The method of claim 19 wherein the transactions include read transactions configured to cause first information to be read from the memory card and write transactions configured to cause second information to be written to the memory card.

28. (Original) A memory card comprising:

a buffer configured to receive transactions;

a storage media;

a clock configured to generate a clock signal and provide the clock signal to the buffer and the storage media;

means for determining a rate of the transactions received by the buffer; and

means for causing the clock signal to be set at a rate associated with the rate of transactions.

29. (Original) The memory card of claim 28 further comprising:

an interface coupled to the buffer;

wherein the interface is configured to receive the transactions from a host device and provide the transactions to the buffer.

30. (Original) The memory card of claim 28 wherein the transactions include read transactions configured to cause information to be read from the storage media.

31. (Original) The memory card of claim 28 wherein the transactions include write transactions configured to cause information to be written to the storage media.

32. (Original) The memory card of claim 28 wherein the transactions include read configured to cause information to be read from the storage media and write transactions configured to cause information to be written to the storage media.

33. (Original) A memory card comprising:

a buffer;

an interface configured to receive transactions from a host device and provide the transactions to the buffer;

a storage media;

a control circuit coupled to the buffer and the storage media; and

a processor system coupled to the control circuit;

wherein the processor system is configured to detect a rate of transactions received by the buffer, wherein the processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the rate of transactions received by the buffer, and wherein the control circuit is configured to cause the first clock signal to be provided to the buffer and the storage media.

34. (Original) The memory card of claim 33 further comprising:

a master clock configured to provide a second clock signal at a second clock rate to the processor system and the control circuit;

wherein the control circuit is configured to generate the first clock signal using the second clock signal.

35. (Original) The memory card of claim 33 wherein the transactions include read transactions configured to cause information to be read from the storage media.

36. (Original) The memory card of claim 33 wherein the transactions include write transactions configured to cause information to be written to the storage media.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.